Summary of Expertise: Digital Front End verification

3 ~ 5 years years of experience

➢ must have: Experience and excellent skills in Gate Level Simulation of Digital Designs, in particular CPU designs - preferably RISC V CPU.

➢ Must have: Synopsys' Tools – DC and VCS - based experience

➢ Knowledge of RISC-V Processor, Instruction Set, Tool chain desirable

➢ Verilog, System Verilog based RTL Design / Verification experience

➢ Experience and Excellent skills in IP, Soc and Processor Level Verification.

➢ Good knowledge on industry standard bus protocols like AXI, AHB and APB.

➢ Experience in Processor Instruction Set Architecture (ISA) Verification.

➢ Good knowledge of module/system level Verification using Hardware Verification Languages.

➢ Hands on experience in writing Test Plans, test cases ,developing verification requirements ,Verification plan at module/system level

➢ Ability to rapidly learn new concepts with excellent interpersonal and problem solving skills.

➢ Be able to mentor a team of Verification engineers for the above activities

Technical Skills

Operating Systems Windows, UNIX. Languages Verilog, SystemVerilog, Hardware Tools Synopsys's VCS, Mentor's Questasim, Programming and Scripting languages